ELECTRONIC COUNTERS

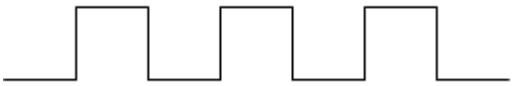
A counter is one of the most useful and versatile systems in digital circuits, which is designed to count the number of clock pulses arriving at its input terminal. Since clock pulses occurs at regular intervals, the counter can be used as an instrument for measuring time and frequency. Counter also performs the jobs like dividing the frequency, addressing and serve as memory unit. Flip flops circuits are the basic block to design or build the counter circuit.

MULTIVIBRATORS:

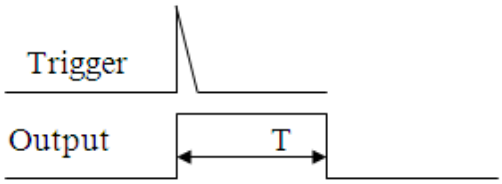
Multivibrator is an electronic circuit whose output oscillates between the low and high state. It is a circuit capable of generating clock pulses. There are three basic modes of multivibrator circuit.

1) Asatable multivibrator
2) Monostable multivibrator
3) Bistable multivibrator

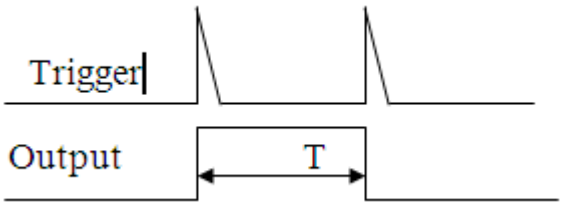
Astable multivibrator: Astable multivibrator is an electronic circuit whose output is continuously oscillates between that of low and high state. This circuit has no stable state and does not require trigger pulse to oscillate the output. Its frequency can be changed and used as clock generator.



Monostable multivibrator: Monostable multivibrator is an electronic circuit that has only one stable state. This circuit changes its output state for the specific time period and requires trigger pulse to change the output, gives one pulse for one trigger. Used as timer.



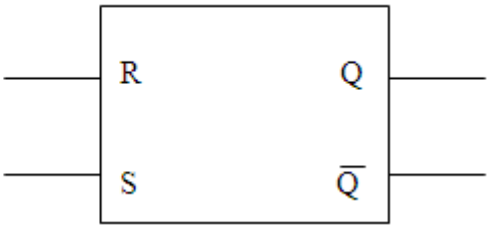
Bistable multivibrator: Bistable multivibrator is an electronic circuit that has two stable states. The circuit remains indefinitely in the state till the next trigger pulse is applied. For every change it takes separate trigger, gives one pulse for two input triggers. Used as flip flop, counter, memory cell, latch etc.



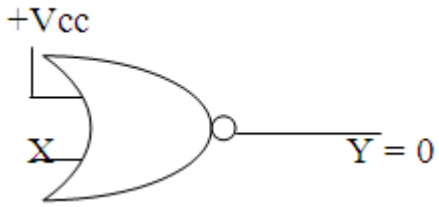
Flip Flops: Flip flop is a bistable multivibrator known as 'latch' it plays an important role in registers, counters and memory circuits. Flip means logical 1 state known as 'set' and Flop means logical 0 state is known as 'reset'.

R - S Flip Flop – It is a basic circuit, which requires other to construct other flip-flop. It has two inputs S and R and two outputs Q and $\overline{Q}$ known as normal output and complimentary output.

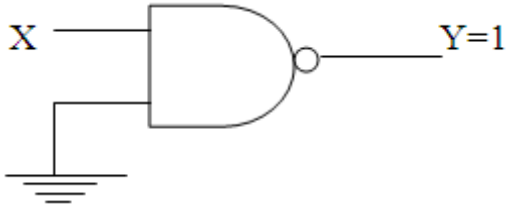
R	S	Q	$\overline{Q}$
0	0	N/C	
0	1	1	0
1	0	0	1
1	1	Race	



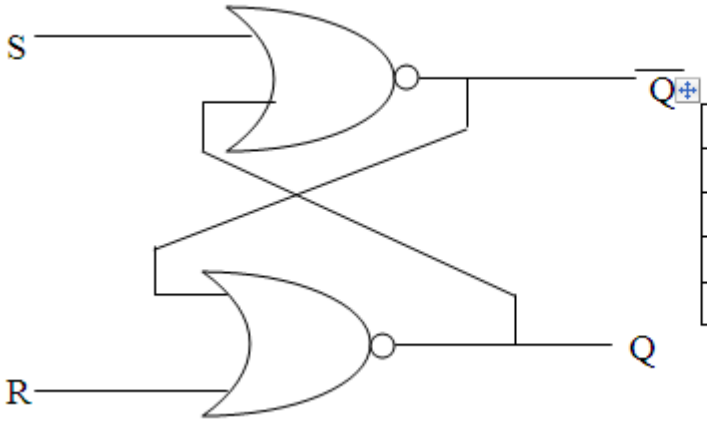
Disable state – When one of the input of the NOR gate is known and it is 1, then irrespective of other input output is always 0 or output is said to be 'disabled'.



Enable state – When one of the inputs of the NAND gate is known and it is 0, then irrespective of the other input output is always 1or output is said to be 'enabled'.



R - S Flip Flop using NOR gate – This type of the flip flop can be constructed with the help of two NOR gates by coupling to each other that is output of one gate is connected to the input of the other and output of other is connected to the first gate.



R	S	Q	$\overline{Q}$
0	0	N/C	N/C
0	1	1	0
1	0	0	1
1	1	Race	Race

Working –

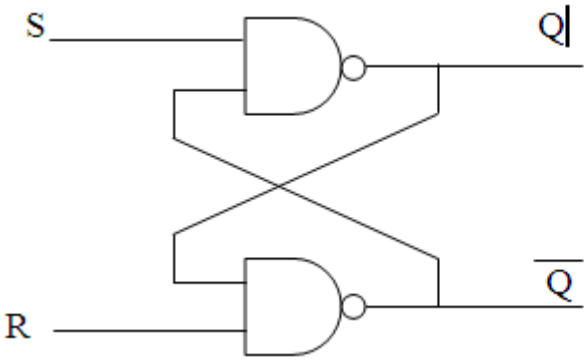
1) When S = 0, R = 1 lower NOR gate is disabled and upper NOR gate is enabled which will produce Q = 0 & $\overline{Q}$ = 1. This condition is known as reset condition.

2) When S = 1, R = 0 upper NOR gate is enabled and lower NOR gate is disabled which will produce Q = 1 & $\overline{Q}$ = 0. This condition is known as set condition.

3) When both S = R = 1 upper & lower NOR gate is disabled but practically there is race between them we can not determine the output state, output may be set or reset and hence called as Race / forbidden condition.

4) When both S = R = 0 upper & lower NOR gates does not change there states, they remain in the same state or in the last state called as No Change (N/C).

R - S Flip Flop using NAND gate – This type of the flip flop can be constructed with the help of two NAND gates by coupling to each other that is output of one gate is connected to the input of the other and output of other is connected to the first gate.



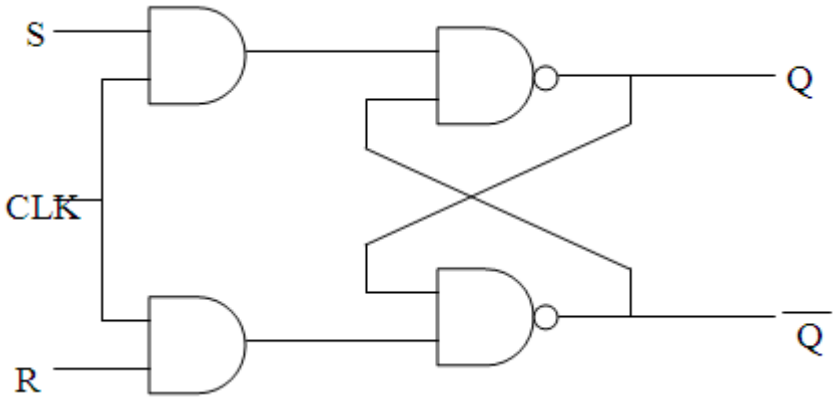
R	S	Q	$\overline{Q}$
0	0	Race	Race
0	1	1	0
1	0	0	1
1	1	N/C	N/C

Working – Working same as NOR gate as R-S flip flop by using 'enabled state' of NAND gate.

Clocked R – S Flip Flop – Practically a control input is required in addition to the R & S inputs to operate the flip flop. The common control signal is called as 'CLOCK'

When clock is 0, then irrespective of R & S inputs the flip flop remains disabled or there is no change in the output. It is indicated by X in the truth table known as 'don't care' condition.

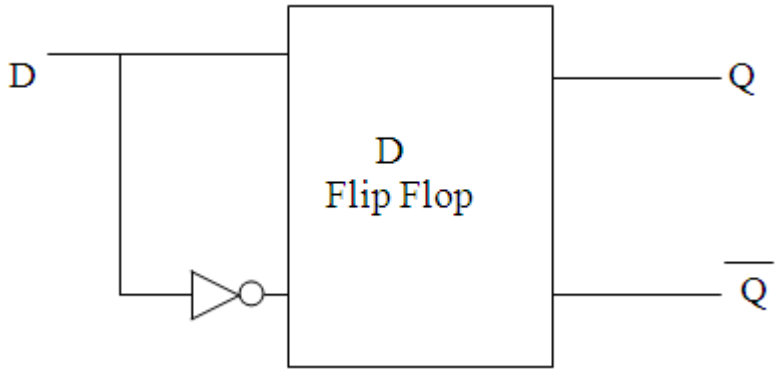
When clock is 1, then flip flop works its normal operation.



CLK	R	S	Q	$\overline{Q}$
0	X	X	N/C	N/C
1	0	0	N/C	N/C
1	0	1	1	0
1	1	0	0	1
1	1	1	Race	Race

D Flip Flop – The R- S flip-flop has two drawbacks 1) It requires two separate inputs R & S, 2) The possibility of race or forbidden condition. Both drawbacks are eliminated in D flip flop. This flip-flop has only one input terminal called as data input.

When D = 1 then Q = 1 & when D = 0 then Q = 0



D	Q	$\overline{Q}$
0	0	1
1	1	0

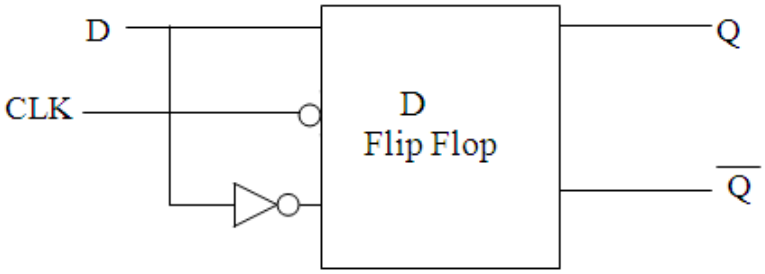
Clocked D Flip Flop – The R- S flip-flop has two drawbacks 1) It requires two separate inputs R & S & 2) The possibility of race or forbidden

condition. Both drawbacks are eliminated in D flip flop. This flip-flop has only one input terminal called as data input along with control terminal called as clock input.

When CLK = 0 & D = X then Q = N/C and Q = N/C known as 'don't care' condition.

When CLK = 1 & D = 1 then Q = 1 and Q = 0 called as 'set' condition

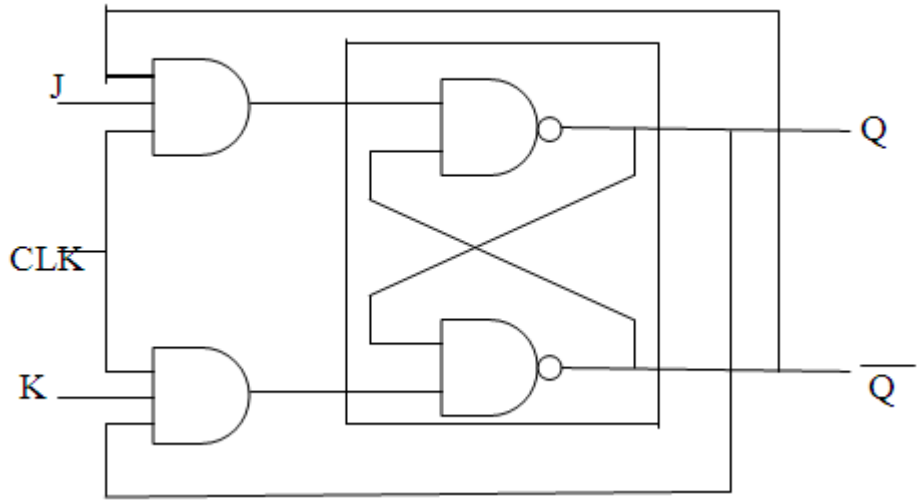
When CLK = 1 & D = 0 then Q = 0 and Q = 1 called as 'reset' condition



CLK	D	Q	$\overline{Q}$
0	X	N/C	N/C
1	0	0	1
1	1	1	0

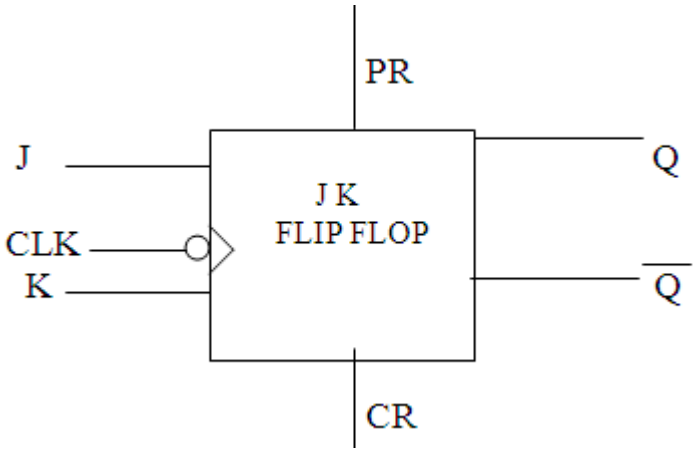
J – K Flip Flop –

This flip flop plays an important role in counter circuits. To build this flip flop, it requires R-S flip flop. When J = K = 1 the output is in 'toggle' mode where toggle means change to opposite state that is at every clock input pulse output changes to opposite state. The J – K flip flop has two additional terminals known as PR & CR (preset & clear) The PR terminal is used to set the output independent of J, K & CLK. CR terminal is used to reset the output independent of J, K & CLK.



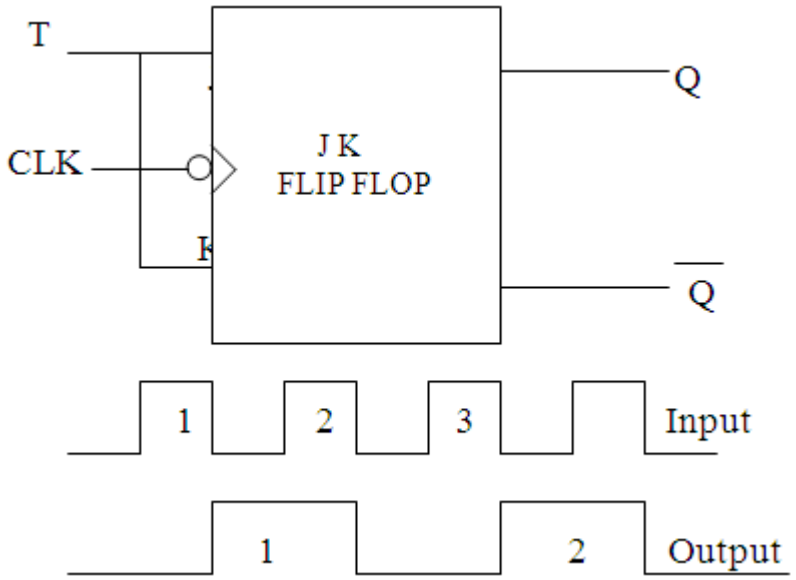
CLK	J	K	Q	Q̄
0	X	X	N/C	N/C
1	0	0	N/C	N/C
1	0	1	1	0
1	1	0	0	1
1	1	1	Toggle	

Block Diagram-



When J- K flip flop is used in counter circuit, it is operated with edge triggering technique. The clock input pulse is positive edge or negative edge type. In positive edge type the output changes at the rising edge of the clock signal or from 0 to 1. In negative edge type the output changes at the falling edge of the clock signal or from 1 to 0.

T Flip Flop – When J-K flip flop permanently connected to the toggle mode it is called as toggle or T flip flop. It has only one input terminal, it is also called as divide by two circuits. Two input pulses are required to get one clock pulse.



Master Slave J - K Flip Flop –The cascaded circuit of two J – K flip flop is called as master slave J-K flip flop. The first flip flop is called as master, it is positive edge triggered type and second flip flop is called as slave, it is negative edge triggered type. The master first initialize the output at positive edge of the input clock pulse during this time slave is in off condition, at the negative edge master is off and slave becomes on that is slave copies the master.

